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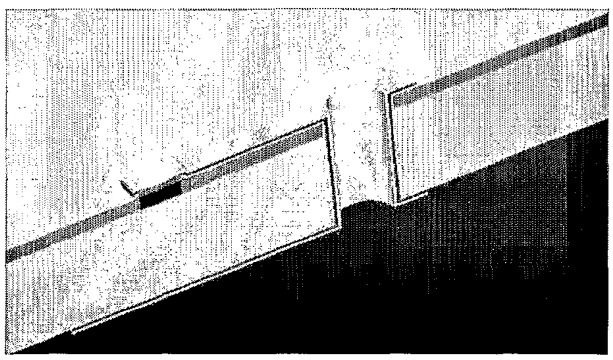
(54) Title: THROUGH WAFER VIA PROCESS AND AMPLIFIER WITH THROUGH WAFER VIA



(57) Abstract: The invention concerns a process for generating a through wafer via from a first to a second external surface of a CMOS or similar circuitry containing wafer, whereby a metal layer is deposited on the second surface of the wafer and where a DRIE process is subsequently used to generate the hole through the wafer material from the first surface to the metal layer and using the metal layer as an etch stop, and whereafter an electrical insulation layer is deposited on the side walls of the hole and an electrically conducting material is provided on top of the electrical insulation material.

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TITLE

Through wafer via process and amplifier with through wafer via.

AREA OF THE INVENTION

The invention concerns a process for generating a feed-through in a semiconductor wafer, which has electric circuitry embedded in a first surface. The embedded circuitry could be a CMOS or similar electronic device. The invention further concerns an amplifier comprising electric circuitry embedded in a first side of a semiconductor wafer and a feed-through from the first to a second side of the semiconductorwafer

BACKGROUND OF THE INVENTION

Amplifiers are produced on wafers and singulated after production. It has been proposed to mount separate electronic components directly on the wafer prior to singulation of the individual amplifiers. This technique is space saving as it becomes possible to omit the printed circuit board, as all components for driving the amplifier can be placed on the surface of the integrated circuit embedded in the silicon wafer. In some cases it is a problem to provide sufficient space also for the bond pads for in/out signals and for power supply for the IC on the surface when also the electric components are placed here. In this case it would be advantageous to be able to either place the bond pads or the electric components on the opposite side of the silicon wafer with the embedded IC. This requires electric leads or vias connecting the two sides of the semiconductor wafer. In the following such an electric conducting path leading through the wafer material from one to the other side thereof is called a feed-through or a via. The via or feed-through comprises a hole all the way through the wafer material, an insulation layer covering the inside surface of the hole and electrically conducting material preferably metal. In this way an electrically leading path from the one to the other side of the wafer is created which is electrically isolated from the other parts of the wafer.

Application of through-wafer via technology further offers the possibility of advanced microelectronic chip stacking or stacking of various types of microcomponents directly on for example a CMOS chip. The latter implies the possibility of stacking e.g. MEMS-

devices on CMOS chips in order to provide the often needed direct conditioning of the MEMS device output signal. If through-wafer vias is applied in combination with wafer level packaging, fabrication of ultra small 3-D packages containing several active devices is possible. Ultimately this 3-D package could represent a complete microsystem that could be surface mounted as a ball grid array (BGA) using solder bumps.

In previous suggested processes schemes to generate through-wafer vias in a dry etch process it has been a problem that notching occurs at the etching step

SUMMARY OF THE INVENTION

The purpose of the invention it to present a simple process for post processing of high aspect ratio through-wafer vias in CMOS wafers. According to the invention a process for through-wafer via fabrication is suggested, that has a realistic chance of being successfully implemented in a high-end portable product. The leading thoughts behind the process design is to create a process sequence containing as few critical process steps as possible, and to create a process sequence that is relatively insensitive to process variations and non-uniformities. The resulting process design according to the invention allows great latitude in the choice of parameters for the individual process steps, thus lightening the task of transferring the final process from development to production facility.

The through-wafer via process presented is designed to be applicable as a post process to any kind of CMOS wafer regardless of the type of passivation provided by the CMOS foundry (usually silicon oxide, silicon nitride or polyimide). The thermal budget of a CMOS compatible process is rather limited, i.e. normally below ~450°C (above this approximate temperature the CMOS Al metallization will start diffusing into the silicon, thus causing non-functional circuits). For post processing on CMOS wafers having polyimide passivation the thermal budget is reduced even further. Thus, in present case the highest process temperature has been kept at 300°C.

The process developed offers simple but well controlled through-wafer via formation eliminating common problems like notching and poor distribution of via metallization and insulation material.

The fast Si-DRIE process offers high etch rates in the range of 6 μm/min. depending on actual loading, feature sizes and etch depth.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a 3-D illustration of a final through-wafer via providing electrical contact from a CMOS pad on the front side of the chip to a redistribution network on the backside.

Fig. 2 is a simplified process sequence for processing of a through-wafer via in a CMOS wafer.

Fig. 3 is a cross sectional illustration of a through-wafer via fabricated using a metal layer provided as an inherent part of the CMOS wafer as an etch stop.

DESCRIPTION OF A PREFERRED EMBODIMENT

The through-wafer via process presented is designed to be applicable as a post process to any kind of CMOS wafer regardless of the type of passivation provided by the CMOS foundry (usually silicon oxide, silicon nitride or polyimide). The thermal budget of a CMOS compatible process is rather limited, i.e. normally below ~450°C (above this approximate temperature the CMOS Al metallization will start diffusing into the silicon, thus causing non-functional circuits). For post processing on CMOS wafers having polyimide passivation the thermal budget is reduced even further. Thus, in present case the highest process temperature has been kept at 300°C.

The process developed offers simple but well controlled through-wafer via formation eliminating common problems like notching and poor distribution of via metallization and insulation material. The process is based on fast Si-DRIE of wafer through-holes, low temperature deposition of through-hole insulation, double sided sputtering of Cr/Au, and electroless deposition of Cu. The fast Si-DRIE process offers high etch rates in the range of 6 μm/min. depending on actual loading, feature sizes and etch depth.
A 3-D illustration of a final through-wafer via is shown in Figure 1.

A simplified version of the process sequence is shown in Figure 2.

The process sequence is applied directly on the CMOS wafer 1 as provided by the CMOS foundry (backlapped). Initially a protective PECVD silicon nitride layer 2 is deposited on the front side of the wafer (Figure 2, a). The CMOS wafer 1 is then chemical mechanical polished (CMP) in order to obtain a smooth and defect free surface suitable for further processing. The protective PECVD nitride 2 covering the entire front surface has to be opened above the CMOS contact pads 3 in order to allow subsequent deposited metal layers to make electrical contact to the pads 3. The PECVD nitride 2 is patterned in a reactive ion etching (RIE) process using a suitable photoresist mask.

A sacrificial Al layer 4 is sputter deposited on the backside of the wafer (Figure 2, b) in order to provide an etch stop for the DRIE formation of the wafer through-holes (Figure 2, d). Additionally, the Al etch stop 4 functions as a membrane preventing He leaking into the process chamber once the wafer 1 through-holes are formed (He is used for wafer cooling during Si-DRIE). In present case an Al thickness of 2 μm has been chosen in order to provide a sufficient mechanically stable etch stop layer. Other materials than Al can be used for the purpose of a conductive etch stop layer. The choice of material may depend on the specific rules and requirements of the production facility.

In a further embodiment of the invention the etch stop layer can be provided as an inherent part of the CMOS wafer such as a bond pad or as a buried metal layer (Figure 3, 20). In this embodiment DRIE formation of the via holes will be performed from the backside of the CMOS wafer using a bond pad or a buried metal layer near the CMOS

wafer front surface as an etch stop. In this case removal of a sacrificial etch stop layer can be avoided.

A thick photoresist layer 5 (9.5 μm) is deposited on the front side of the wafer 1. The photoresist 5 is patterned to define circular openings 6 with a diameter of 100 μm. The PECVD silicon nitride 2 is then patterned correspondingly using RIE with the photoresist acting as a mask (Figure 2-c). The wafer through-holes 7 are formed in a room temperature Si-DRIE process (Figure 2, d) using alternating gas chemistry; SF_6 for Si etching and C_4F_8 for intermediate passivation (BOSCH process). The Si-DRIE process terminates on the Al layer 4 on the backside of the wafer 1 without deteriorating the profile of the wafer through-hole 7, i.e. without notching effects.

After through-hole formation the sacrificial Al etch stop layer 4 is etched using a mixture of phosphoric, acetic and nitric acid. The resulting etch rate is approximately 0.2 μm/min.

The wafer through-holes 7 are insulated by room temperature CVD of 3 μm Parylene C (poly-monochloro-para-xylylene) 8 (Figure 2,e). The Parylene C CVD process is characterized by the ability to coat the entire wafer conformably in one process step. The simultaneous coating of wafer front, backside and inside of wafer through-holes provides an efficient insulation of the final via. Alternatively the wafer through-holes can be insulated using a low temperature CVD process for deposition of a silicon based dielectric material such as silicon oxide, silicon nitride or silicon oxynitride. The preferred alternative to CVD deposited parylene is PECVD deposition of silicon oxide based on a TEOS precursor.

The Parylene 8 deposited on the CMOS contact pads 3 on the wafer front side is removed in a RIE process using a standard photoresist layer as a mask (Figure 2, e). The small lateral dimension of the via holes 7 combined with the mild resolution requirement (only definition of large feature sizes is needed) allows for spinning of photoresist in a standard photoresist spinner.

Prior to deposition of the through-hole metallization the Parylene surface is treated in a mild oxygen plasma in order to improve the conditions for obtaining good metal adhesion.

The through-hole metallization is deposited immediately after the plasma treatment. A plating base 9 consisting of 500 nm Cr and 500 nm Au is sputter deposited on both sides of the wafer (Figure 2-f).

In order to obtain sufficiently low resistance of the final through-wafer vias a thick Cu-layer 10 is deposited (3-5 μm). The Cu 10 is deposited in an electroless process using the sputter deposited Cr/Au as a seed layer (Figure 2-g), i.e. simultaneous deposition on both sides of the wafer and inside the wafer through-holes.

In a further embodiment the through-hole metallization is deposited by means of low temperature metal organic chemical vapour deposition (MOCVD). Preferably MOCVD TiN is deposited as an adhesion layer providing good adhesion to the through-hole insulation material, and MOCVD Cu is subsequently deposited in order to provide low electrical resistance of the through wafer via. Alternatively the MOCVD TiN and MOCVD Cu process can be followed by electrochemical deposition of Cu in order to further increase the via metal thickness and thereby further decrease the electrical resistance of the through-wafer via. Preferably electrochemical deposition of Cu is either performed as an electroless process or as a pulse reverse plating process.

In order to define the final structure of the via metallization on front and backside of the wafer an electrodeposited, negatively working photoresist 11 is applied. By applying a DC voltage across the Cr/Au/Cu metallization the resist is uniformly deposited all over the wafer (including inside of wafer through-holes) in a cataphoretic electrodeposition process taking place at 35°C (Figure 2-h). This type of resist is not widely used within the field of MEMS, though it is well known in the printed circuit board (PCB) industry as it is originally developed for patterning of Cu wires on PCB. Using a standard mask aligner the front and backside of the photoresist coated wafer is exposed, and the electrodeposited resist is subsequently developed in a dedicated developer. Alternatively

an electrodeposited, positively working photoresist can be used, however the negative tone photoresist is preferred as it is more chemically stable.

Finally, the through-wafer via metallization is structured by wet chemical etching using the electrodeposited photoresist as an etch mask (Figure 2-i). The Cu metal is etched using a sodium persulfate solution, whereas the underlying Cr/Au base layer is sequentially etched using commercial Au and Cr etchants, which are both Cu compatible.

The electrodeposited photoresist mould is stripped using a dedicated remover (Figure 2-j).

In order to make the final through wafer via applicable for a commercial application it needs to be passivated. The passivation layer protects the through wafer via from corrosion and wear. The deposited passivation material has to be patterned above input/output terminals in order to allow for external electrical contact to the CMOS chip with integrated vias. Additionally the passivation layer can have a vital function in the packaging of the device. The passivation layer can e.g. function as a construction material in the process of fabricating solder bumps. The passivation layer can be provided by spinning of a polymer material such as BCB (benzocyclobutene) or preferably by CVD deposition of parylene.

CLAIMS

1. Process for generating a through wafer via from a first to a second external surface of a CMOS or similar circuitry containing wafer, whereby a metal layer is deposited on the second surface of the wafer and where a DRIE process is subsequently used to generate the hole through the wafer material from the first surface to the metal layer and using the metal layer as an etch stop, and whereafter an electrical insulation layer is deposited on the side walls of the hole and an electrically conducting material is provided on top of the electrical insulation material.

2. Process as claimed in claim 1, whereby the metal layer is provided as an inherent part of the CMOS or similar circuitry containing wafer.

3. Process as claimed in claim 1, whereby the metal layer is a dedicated etch stop layer which subsequently is removed.

4. Process as claimed in claim 3, whereby the metal layer is deposited by sputtering.

5. Process as claimed in claim 1, whereby low temperature deposition of through-hole insulation, is accomplished by the use of a room temperature CVD process for deposition of a polymer material.

6. Process as claimed in claim 5, whereby the polymer used in the CVD process is of the type parylene.

7. Process as claimed in claim 6, whereby the polymer used in the CVD process is poly-monochloro-para-xylylene also known as parylene C.

8. Process as claimed in claim 1, whereby low temperature deposition of through-hole insulation, is accomplished by the use of a low temperature CVD process for deposition of a silicon based dielectric material, preferably a PECVD TEOS oxide.

9. Process as claimed in claim 5-8, whereby double sided sputtering of Cr/Au on the insulation material layer in order to gain electrical contact through the via.

10. Process as claimed in claim 9, whereby subsequent deposition of Cu is conducted in order to decrease the electrical resistance of the through wafer via.

11. Process as claimed in claim 10, whereby Cu is chemically deposited in an electroless deposition process.

12. Process as claimed in claim 10, whereby Cu is deposited in an electroplating process, preferably using pulse reversal.

13. Process as claimed in claim 5-8, whereby a MOCVD process is used for deposition of TiN on the insulation material and a MOCVD process subsequently used for deposition of Cu in the through hole for generating an electrical conducting path through the hole.

14. Amplifier produced according to one ore more of the claims 1-13, wherein terminals for gaining contact with the CMOS structure embedded in the surface of a front side of semiconductor wafer are placed on both back and front sides of the wafer and where a through wafer via connects the terminals on the back side with the CMOS circuitry embedded in the front side of the wafer.

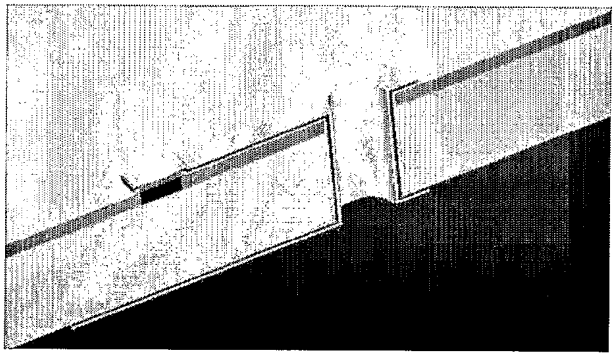

Fig. 1

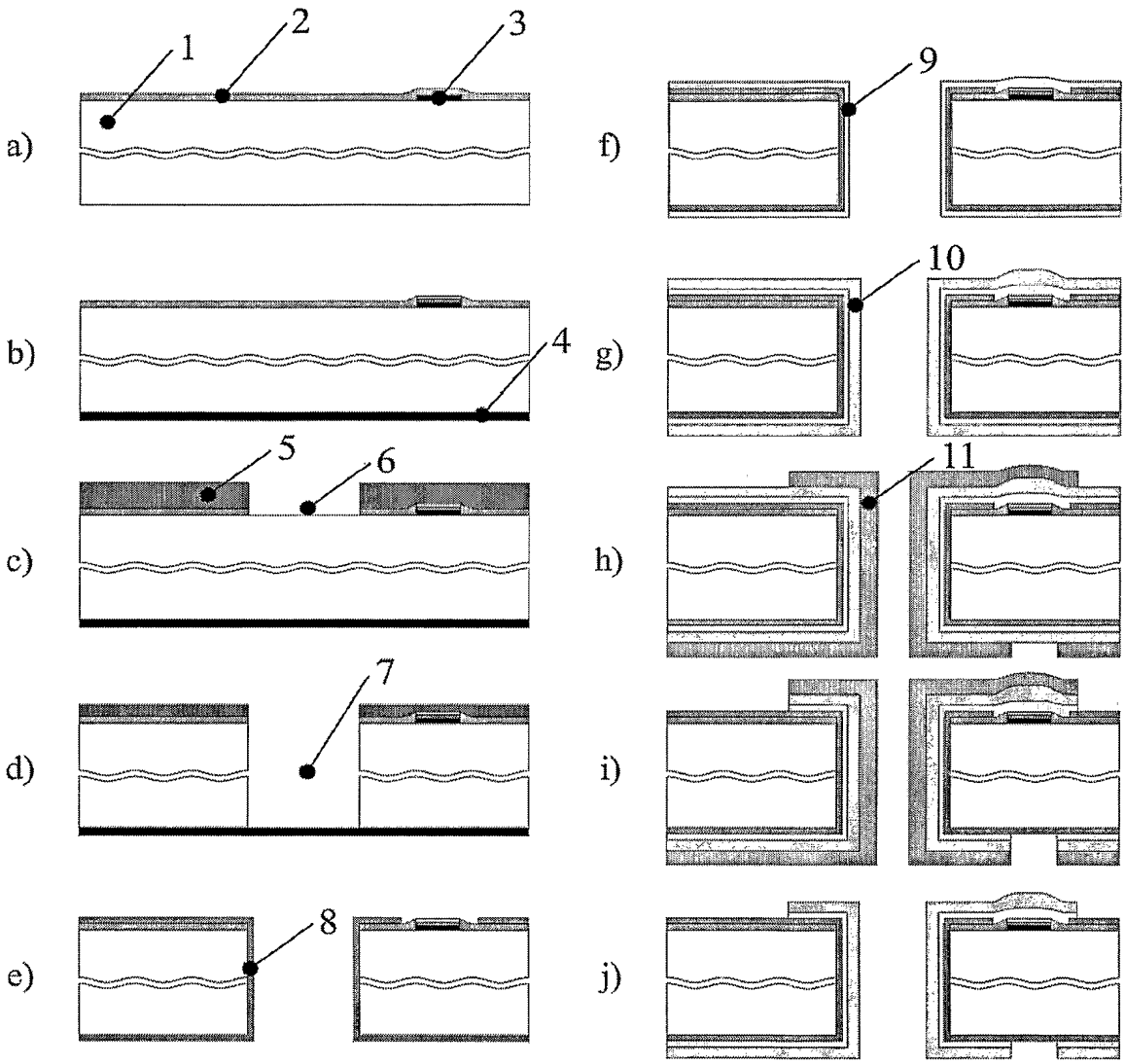

Fig. 2

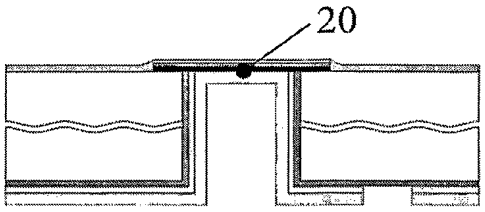

Fig. 3